Shashank Nag

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Education

The University of Texas at Austin *Fall 2023 - ongoing*

Ph.D. in Electrical and Computer Engineering; ***GPA: 4.0/4.0***

Research Focus: Hardware Accelerators for Machine Learning, Hardware-efficient high throughput LLMs, Weightless Neural Networks

Advisor: Prof. Lizy K John

Indian Institute of Technology Madras *May 2023*

Bachelor of Technology in Electrical Engineering; ***CGPA: 9.34/10.0***

Awards & Honors

- Awarded the IIT Madras Young Research Fellowship for 2021, as a part of the 30-membered cohort selected from the undergraduate class.
- Selected for the Indo US Science & Technology Forum - Viterbi Research Experience Program, among 15 students selected from across India.
- Secured an All India Rank of 336 in the Joint Entrance Examination (Advanced) 2019 among 0.15 million candidates.
- Awarded the KVPY scholarship, a National Research Fellowship by the Indian Institute of Science Bengaluru.
- Inducted to IEEE Eta Kappa Nu (HKN) Electrical & Computer Engineering Honor Society at The University of Texas at Austin.

Publications & Presentations

- **Shashank Nag,** Logan Liberty, Aishwarya Sivakumar, Neeraja J. Yadwadkar, and Lizy K. John, "Lightweight Vision Transformers for Low Energy Edge Inference", ML for Computer Architecture and Systems (MLArchSys) Workshop 2024, colocated at the IEEE International Symposium on Computer Architecture (ISCA) 2024, Buenos Aires, Argentina
- **Shashank Nag*,** Zachary Susskind*, Aman Arora, Allan T.L. Bacellar, Diego L.C. Dutra, Igor D.S. Miranda, Krishnan Kailas, Eugene B. John, Mauricio Breternitz Jr., Priscila M. V. Lima, Felipe M. G. Franca and Lizy K. John, "LogicNets vs. ULEEN : Comparing two novel high throughput edge ML inference techniques on FPGA", IEEE 67th International Midwest Symposium on Circuits and Systems (MWSCAS) 2024, Springfield, MA. *(*Equal Contribution)*
- **Shashank Nag,** Gourav Datta, Souvik Kundu, Nitin Chandrachoodan, and Peter A. Beerel, "ViTA : A Vision Transformer Inference Accelerator for Edge Applications", IEEE International Symposium on Circuits and Systems (ISCAS) 2023, Monterey, CA
- **Shashank Nag,** "Quasi Weightless Vision Transformers", Poster Presentation, UT Austin iMAGiNE Consortium Symposium 2024

Services

- Served as a reviewer for the 37th International Conference on VLSI Design and 23rd International Conference on Embedded Systems (VLSID 2024), Kolkata, India

Research Experience

Laboratory for Computer Architecture, The University of Texas at Austin Austin, TX

Advisor : Prof. Lizy K John *Aug 2023 -*

Hardware Efficient Machine Learning

- Investigating algorithm-hardware co-design techniques for Machine Learning algorithms, particularly focusing on transformer models
- Incorporated LUT based weightless layers in the Vision Transformer, achieving $\sim$ 50% reduction in MAC operations for a small accuracy drop.

IIT Madras & University of Southern California Chennai / Los Angeles

IUSSTF Viterbi Scholar & Bachelor's Thesis | Guides : Prof. Nitin Chandrachoodan & Prof. Peter A. Beerel *May 2022 - Aug 2023*

Hardware Accelerators for Vision Transformers' inference on the edge

- Designed in RTL and implemented a hardware accelerator supporting inference of vision transformers, targeting edge computing FPGAs.
- Optimized the design for resource constrained devices, with 90%+ hardware utilization, eliminating repeated off-chip memory accesses.
- Investigated and proposed a mixed precision quantised model and an accelerator co-design, optimising on resources and power.

Chair of Integrated Digital Systems & Circuit Design, RWTH Aachen University Aachen, Germany

DAAD WISE Research Internship | Guide : Prof. Dr.-Ing. Tobias Gemmeke & Christian Lanius *Jun 2022 - Jul 2022*

Hardware Accelerator for minimap2 algorithm

- Analysed the minimap2 algorithm for genome alignment, and identified key bottlenecks and sections suitable for hardware implementation.
- Designed and implemented in SystemVerilog, a modified Systolic Array based hardware accelerator design on the target Xilinx ZCU106 FPGA.

RISE Lab, IIT Madras Chennai, India
Shakti Open Source RISC-V Processor Development Program | Guide : Prof. Kamakoti V *Aug 2021 - March 2023*

Shakti-on-Shakti SoC implementation on FPGAs

- Deployed the Shakti SoC design onto the Aldec TySOM3A FPGA board, and performed end-to-end emulations and tests.
- Added DDR4 & ethernet support to the SoC by interfacing Xilinx IP cores using Bluespec SystemVerilog wrappers.
- Built the AXI4 Stream fabric in Bluespec SystemVerilog based on the AMBA 4 AXI-Stream specifications

GalaxEye Space Chennai, India
Embedded Systems Research Intern | Guide : Rakshit Bhatt *May 2021 - Jul 2021*

Image Processing for Edge Computing

- Performed literature review on Hyperspectral Image Preprocessing Algorithms, and implemented an optimised version of SOTA algorithm.
- Deviced a novel method to georeference hyperspectral images aided by the SAR imagery available on the same satellite.
- Analysed and developed a pipeline for deploying radiation tolerant embedded electronic devices for space applications.

Notable Projects

Custom Cache Replacement, Branch Prediction & Data Prefetching Policies IIT Madras
Computer Architecture : Course Project *Jul - Nov 2022*

- Designed, implemented and benchmarked a cache replacement policy based on Reuse Distance Prediction using the Champsim framework.
- Implemented and evaluated the performance of a range of ML / perceptron based branch prediction policies.
- Coupled the IP-stride prefetching policy with a distance indexed prefetching policy to enable fast learning of data access patterns.

8-bit Signed Carry Save Multiplier Design and Layout IIT Madras
Digital IC Design : Course Project *Jul - Nov 2022*

- Designed an 8bit×8bit signed carry save multiplier with pareto optimal area and delay. Extended the design into a two-stage pipelined one.
- Performed the layout and analysis of the design using the GNU Electric tool, incorporating shared diffusions and other layout optimisations.

Network-on-Chip Prototype IIT Madras
CAD for VLSI : Course Project *Jul - Nov 2021*

- Implemented a two level Network-on-chip prototype over a range of network topologies using Bluespec SystemVerilog.
- Implemented a low-latency node architecture incorporating VC based routers and arbiters, while preventing deadlocks and livelocks.
- Developed a customizable instantiation of the entire design for user specified topologies, and simulated the operation of NoC using cocotb.

RISC-V 32 Single Cycle CPU Design IIT Madras
Computer Organization : Course Project *Jul - Nov 2021*

- Designed a single-cycle RISC-V 32-bit CPU using Verilog and performed its hardware implementation on the Pynq Z1 FPGA board.

Teaching Experience

The University of Texas at Austin Austin, TX
Teaching Assistant for Capstone Design under Prof. Leonard (Frank) Register *Fall 2023 & Spring 2024*

- Guided senior undergrad student teams working on a wide range of Capstone Design projects.
- Held weekly reviews to monitor progress and provide insights on possible directions and innovations.

Indian Institute of Technology Madras Chennai, India
Teaching Assistant for EE2003 Computer Organization Course under Prof. Nitin Chandrachoodan *Fall 2022*

- Setup verilog assignments, organized lab sessions & hardware demonstrations, and evaluated the students enrolled in the course.
- Closely guided and mentored a group of 7 students in the course, holding periodic discussions and feedback sessions.

Coursework & Labs

- Computer Performance Evaluation and Benchmarking
- Computer Architecture
- CAD for VLSI Systems
- Analog IC Design
- Digital Design with PLDs and FPGAs *

Computer Organization
Mapping DSP Algorithms to Architectures
Probability Foundations, Linear Algebra
Machine Learning for Engineering & Science *

ML for Systems & Systems for ML
Digital IC Design
Digital Systems Testing & Testable Design
High Speed Computer Arithmetic
Data Structures and Algorithms *

* : Audited MOOC

Skills

- **Programming Languages**: C, C++, Python, HTML
- **Tools**: Xilinx Vivado, Xilinx Vitis HLS, MATLAB, LTSpice, Verilator, cocotb, LaTeX

HDLs: Verilog, SystemVerilog, Bluespec SystemVerilog
Technologies: RISC-V, AVR/ARM Assembly, PyTorch/TF

Extra Curricular Activities

- Pursuing Indian Classical Music & Tabla instrumental recital, with a strong affinity towards Indian heritage.
- Involved in inter-school debates, elocutions & extempore competitions with well-honed public speaking skills. Interviewed Nobel laureate Dr. Barry Barish, Dr. Raghuram Rajan, Dr. Madhavan Nair, & Dr. K. Radhakrishnan as a part of our Institute's annual technical festival.

Science Communication | Leadership | Volunteering

- Initiated the EE Research Club at IIT Madras that engages in instilling research culture amongst undergrads through weekly sessions.
- Initiated and led the production of a series of informative videos on popular science topics, including 5G, Space Technology and Pandemics.
- Convened the Classical Arts Club at IIT Madras during 2020-21, leading a smooth transition to virtual activities from on-ground events.
- Led a team of 6 students to organize the Spotlight Lecture Series, featuring the likes of Prof. David Patterson, and Nobel laureates.
- Volunteer with SPIC MACAY, a cultural movement aimed at promoting the rich Indian cultural heritage globally among the youth.
- Volunteered for the "Each One, Reach One, Teach One" National Adult Literacy Mission by Rotary India by conducting classes for house helps.