Shashank Nag

: shashank@smail.iitm.ac.in | : shashanknag | : shashank-nag | : shashanknag.github.io

Education

Indian Institute of Technology Madras *Expected May 2023*

Bachelor of Technology in Electrical Engineering; ***CGPA: 9.27/10.0***

Scholastic Achievements

- Awarded the IIT Madras Young Research Fellowship for 2021, as a part of the 30-membered cohort selected from the undergraduate class.
- Selected for the IUSSTF - Viterbi Summer Research Experience Program, among 15 students selected from across India.
- Selected for the DAAD - WISE Research Internship Program, among 150 students selected from across India.
- Secured an All India Rank of 336 in the Joint Entrance Examination (Advanced) 2019 among 0.15 million candidates.
- Secured an All India Rank of 858 in the Joint Entrance Examination (Mains) 2019 among nearly 1 million candidates.
- Awarded the KVPY scholarship, a National Research Fellowship by the Indian Institute of Science Bengaluru, with an All India Rank of 762.
- Secured first position in the Indian state of Maharashtra in the All India Senior Secondary Certificate Examination (CBSE – Grade XII) 2019.

Publications

- **Shashank Nag,** Gourav Datta, Souvik Kundu, Nitin Chandrachoodan, Peter A. Beerel, "Hardware Accelerator for Vision Transformers' inference on the edge"*, *Manuscript under review* at IEEE International Symposium on Circuits and Systems (ISCAS) 2023

  * *Title changed for double-blind review*

Research Experience

IIT Madras & University of Southern California Chennai / Los Angeles

IUSSTF Viterbi Scholar & Bachelor's Thesis | Guides : Prof. Nitin Chandrachoodan & Prof. Peter A. Beerel *May 2022 - ongoing*

Hardware Accelerators for Vision Transformers' inference on the edge

- Designed and implemented a hardware accelerator supporting inference of a range of vision transformers, targeting edge computing FPGAs.
- Optimized the design for resource constrained devices, with 90%+ hardware utilization efficiency, eliminating repeated off-chip memory accesses.
- Currently evaluating the performance of mixed precision quantisation and model pruning on inference accuracy, and modifying the accelerator design to support the same.

RISE Lab, IIT Madras Chennai, India

Shakti Open Source RISC-V Processor Development Program | Guide : Prof. Kamakoti V *Aug 2021 - ongoing*

Shakti-on-Shakti SoC implementation on FPGAs

- Deploying the Shakti SoC design onto the Aldec TySOM3A FPGA board, and performing end-to-end emulations and tests.
- Added DDR4 & ethernet support to the SoC by interfacing Xilinx IP cores using Bluespec SystemVerilog wrappers. Currently working on HDMI & MIPI Camera peripherals.
- Built the AXI4 Stream fabric in Bluespec SystemVerilog based on the AMBA 4 AXI-Stream specifications

Bio Fluids Lab, IIT Madras & Sree Chitra Tirunal Institute for Medical Sciences & Technology Chennai/ Trivandrum

Young Research Fellow | Guides : Prof. Prasad Patnaik BSV & Dr. B Jayanand Sudhir *Oct 2021 - May 2022*

Patient Specific Image Analysis for Cerebral Aneurysms

- Analysed CT-Angio images of patients with cerebral aneurysms, extracted 3-D geometries, and computed morphological parameters of the aneurysms using 3D Slicer & ICEM CFD. Proposed and analysed new parameters having significant correlation with aneurysm rupture status.
- Trained an ML based classifier model to predict rupture status of the aneurysm based on their morphological parameters, with 70% accuracy.

GalaxEye Space Chennai, India

Embedded Systems Research Intern | Guide : Rakshit Bhatt *May 2021 - Jul 2021*

Image Processing for Edge Computing

- Performed literature review on Hyperspectral Image Preprocessing Algorithms, and implemented an optimised version of SOTA algorithm.
- Deviced a novel method to georeference hyperspectral images aided by the SAR imagery available on the same satellite.
- Analysed and developed a pipeline for deploying radiation tolerant embedded electronic devices for space applications.

Notable Projects

Custom Cache Replacement, Branch Prediction & Data Prefetching Policies IIT Madras
Computer Architecture : Course Project *Jul - Nov 2022*

- Designed, implemented and benchmarked a cache replacement policy based on Reuse Distance Prediction using the Champsim framework.
- Implemented and evaluated the performance of a range of ML / perceptron based branch prediction policies.
- Coupled the IP-stride prefetching policy with a distance indexed prefetching policy to enable fast learning of data access patterns.

8-bit Signed Carry Save Multiplier Design and Layout IIT Madras
Digital IC Design : Course Project *Jul - Nov 2022*

- Designed an 8bit×8bit signed carry save multiplier with pareto optimal area and delay. Extended the design into a two-stage pipelined one.
- Performed the layout and analysis of the design using the GNU Electric tool, incorporating shared diffusions and other layout optimisations.

Hardware Accelerator for Banded Smith Waterman Algorithm IIT Madras
Mapping DSP Algorithms to Architectures : Course Project *Jan - May 2022*

- Reviewed the hardware implementations of Genome Sequence Alignment Algorithms from an algorithm-hardware co-design perspective.
- Implemented the paper on Accelerator for Smith Waterman Algorithm by Liao et al. in Verilog. Performed the backtracking phase as well on hardware for an optimised dataflow that involves lower writeback latency when interfaced with a CPU, and benchmarked its performance.

Network-on-Chip Prototype IIT Madras
CAD for VLSI : Course Project *Jul - Nov 2021*

- Implemented a two level Network-on-chip prototype over a range of network topologies using Bluespec SystemVerilog.
- Implemented a low-latency node architecture incorporating VC based routers and arbiters, while preventing deadlocks and livelocks.
- Developed a customizable instantiation of the entire design for user specified topologies, and simulated the operation of NoC using cocotb.

RISC-V 32 Single Cycle CPU Design IIT Madras
Computer Organisation : Course Project *Jul - Nov 2021*

- Designed a single-cycle RISC-V 32-bit CPU using Verilog and performed its hardware implementation on the Pynq Z1 FPGA board.

Hardware Accelerator for a simple Neural Network IIT Madras
Computer Organisation : Course Project *Jul - Nov 2021*

- Designed and implemented a hardware accelerator for a simple two stage Feed Forward Neural Network that classifies MNIST images.
- Implemented a weight stationary PE Array based design, optimally utilizing the resources available on the target FPGA. Interfaced it with the PicoRV32 single cycle CPU core, achieving a 64x speedup over the baseline software design implemented on the same core.

Teaching Experience

Indian Institute of Technology Madras Chennai, India
Teaching Assistant for EE2003 Computer Organisation Course under Prof. Nitin Chandrachoodan *Fall 2022*

- Setup assignments, organised lab sessions & hardware demonstrations, and evaluated the students enrolled in the course.
- Closely guided and mentored a group of 7 students in the course, holding periodic discussions and feedback sessions.

Coursework & Labs

- Computer Organisation
- CAD for VLSI Systems
- Analog IC Design
- Digital Design with PLDs and FPGAs *

Computer Architecture
Mapping DSP Algorithms to Architectures
Probability Foundations, Linear Algebra
Machine Learning for Engineering & Science *

Digital IC Design
Digital Systems Testing & Testable Design
Digital Signal Processing
Data Structures and Algorithms *

* : Audited MOOC

Skills

- **Programming Languages**: C, C++, Python, HTML
- **Tools**: Xilinx Vivado, Xilinx Vitis HLS, MATLAB, LTSpice, Verilator, cocotb, LaTeX

HDLs: Verilog, SystemVerilog, Bluespec SystemVerilog
Technologies: RISC-V, AVR/ARM Assembly, PyTorch/TF

Extra Curricular Activities

- Actively involved in writing travelogues & poetry. Published a poem in the Children's corner of the Fall 2013 edition of the Louisville Review.
- Pursuing Indian Classical Music & Tabla instrumental recital, with a strong affinity towards Indian heritage.
- Involved in inter-school debates, elocutions & extempore competitions with well-honed public speaking skills. Interviewed Nobel laureate Dr. Barry Barish, Dr. Raghuram Rajan, Dr. Madhavan Nair, & Dr. K. Radhakrishnan as a part of our Institute's annual technical festival.

Science Communication | Leadership | Volunteering

- Initiated and led the production of a series of informative videos on popular science topics, including 5G, Space Technology and Pandemics.
- Convened the Classical Arts Club at IIT Madras during 2020-21, leading a smooth transition to virtual activities from on-ground events.
- Led a team of 6 students to organize the Spotlight Lecture Series, featuring the likes of Prof. David Patterson, and Nobel laureates.
- Volunteer at SPIC MACAY, a cultural movement aimed at promoting the rich Indian cultural heritage globally among the youth.
- Volunteered for the "Each One, Reach One, Teach One" National Adult Literacy Mission by Rotary India by conducting classes for house helps.